High Speed BCH(4264,4160) Encode/Decode Core

※code length,message length, and error correct number can be customized by the request

<1.Introduction>

The BCH core is **BCH(4264,4160) encode/deecode engine.**

The core's target is ASIC/FPGA.

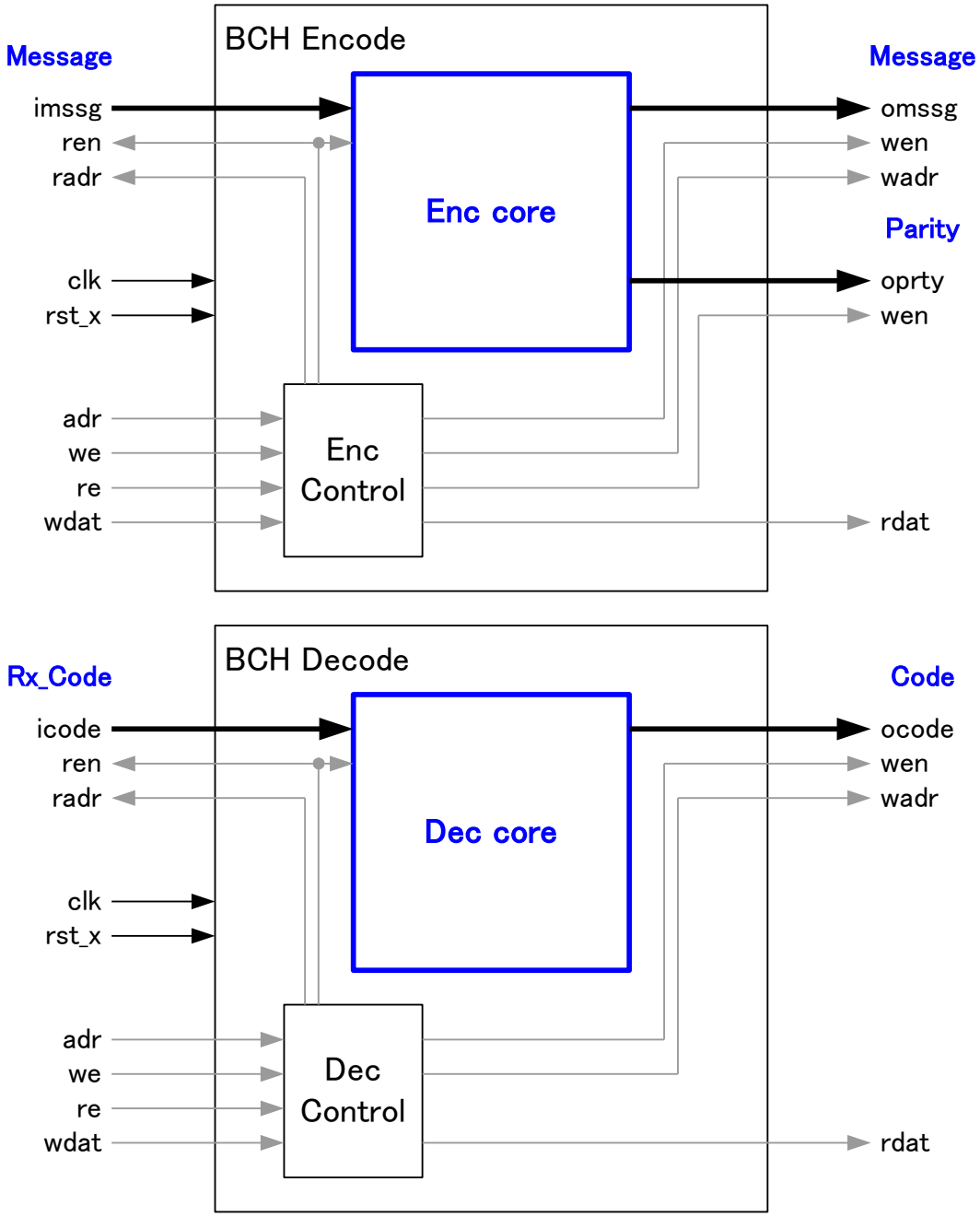
The high performance which achieves the encode/decode throughput **600Mbps** at ASIC / **300Mbps** at FPGA is the feature.

We offer the core module with user interface design.

<2.Features>

The figure below shows a block diagram of the BCH encode/decode system.

The encode/decode cores are shown by the blue encircled modules. (The other modules are user interface.)



-Core Features

- ・Code : based on 8191bit BCH code
  - **BCH(4264,4160) error correct = 8** parity 104bit ※BCH(code length,message lengrh)
- ・Structure : Encode core(ENC)、Decode core(DEC) : 2cores
- ・ENC Process : **560clock** (non-pipelined)
- ・DEC Process : **680clock/1stage x 3 pipeline**
- ・Throughput : ASIC **100MHz clock**
  - ENC : **720Mbps**
  - DEC : **600Mbps**

-User interface Features

<ENC>

- ・Input Data Bus : Message Data Bus **8bit**
- ・Output Data Bus : Message Data Bus **8bit**, Parity Data Bus **104bit**
- ・Registers : - ENC Controll : Start・Busy・Done_flag,Clear
  - Parity : Partiy Data

<DEC>

- ・Input Data Bus : Rx_Code Data Bus **8bit**
- ・Output Data Bus : Corrected Code Data Bus **8bit**
- ・Registers : - DEC Controll : Start・Busy・Done_flag, Clear
  - Error 通知 : Error_number, Error_not_correctable_flag
  - Error Pointer : Error

<ENC/DEC Common>

- ・ Registers : - Registers : Mode setting ,Version, Access check(for Debug)

-System

- ・Clock : Single Synchronous Clock ASIC：**100MHz** FPGA：**50MHz**
- ・Reset : Single Asynchronous Reset
- ・Total pins : **357pin**
- ・RAM : DEC 533index x 8bit x 4
- ・ROM : DEC 8192 x 13bit x 1
- ・Gate size : ENC 10,000gate DEC 80,000gate
- ・Target Technology : ASIC/FPGA

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